

EXAMINATION AND EVALUATION DIVISION
DEPARTMENT OF POLYTECHNIC EDUCATION
(MINISTRY OF HIGHER EDUCATION)

ELECTRICAL ENGINEERING DEPARTMENT

FINAL EXAMINATION
JUNE 2012 SESSION

EE301: ELECTRONIC CIRCUITS

DATE : 19 NOVEMBER 2012 (MONDAY)
DURATION : 2 HOURS (11.15 AM TO 1.15 PM)

This paper consists of **TEN (10)** pages including the front page.

- Section A1 : **Objective (10 Question)**
- Section A2 : **Fill in the blank (10 Question)**
- Section B : **Structured (10 Question)**
- Section C : **Essay (2 Question)**

Answer all questions

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DO NOT OPEN THIS QUESTION PAPER UNTIL INSTRUCTED BY THE CHIEF
INVIGILATOR

(The CLO stated is for reference only.)



SECTION A (20 marks)

Instruction: This section consists of **TEN (10)** multiple choice questions and **TEN (10)** fill in the blanks questions. Write your answers in the answer booklet.

SECTION A1 : OBJECTIVE (10 Questions)

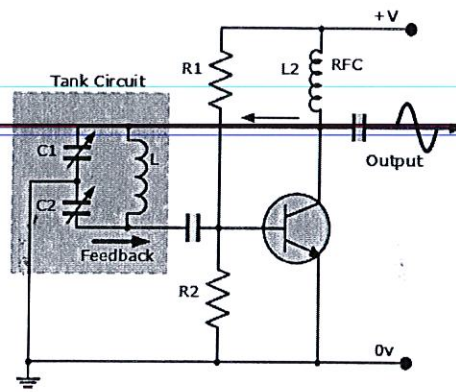
1. *"The circuit is used to reduce the voltage difference to zero or at least to a minimum value."* The statement refers to _____ circuit. [CLO 1]

- A. Transformer
- B. Rectifier
- C. Filter
- D. Regulator

2. The 78XX-09 produces a regulated output voltage of _____. [CLO 1]

- A. 9V
- B. 12V
- C. 15V
- D. 5V

3.



[CLO 1]

Figure 1

Figure 1 shows an oscillator using the LC-tuned circuit. What is the name of the oscillator?

- A. Hartley Oscillator
- B. Armstrong Oscillator
- C. Colpitts Oscillator
- D. Phase-shift Oscillator

4. _____ build a multistage connection.

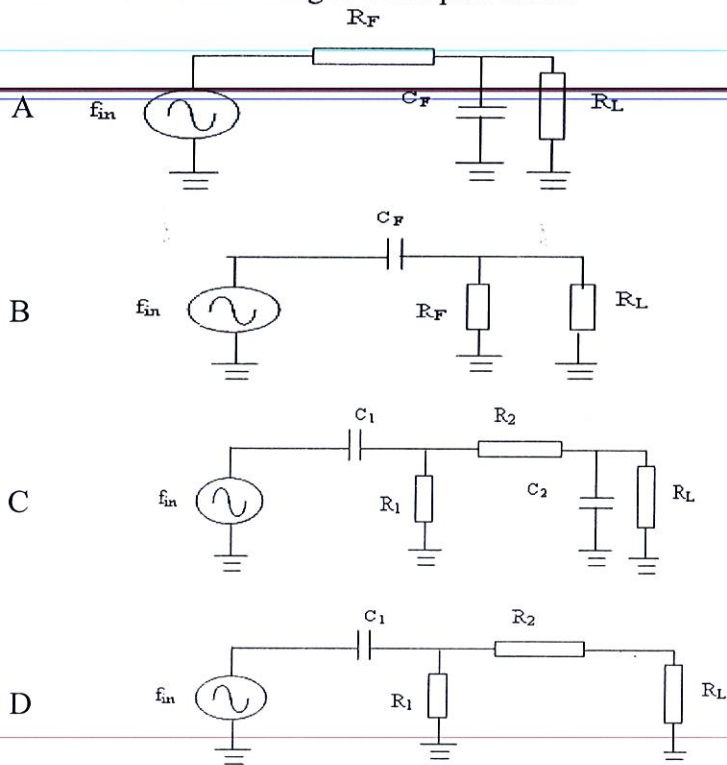
[CLO 1]

- A. Only an inverting Operational Amplifier (OP-AMP) circuit can be used to
- B. Only a non-inverting Operational Amplifier (OP-AMP) circuit can be used to
- C. Both inverting and non-inverting Operational Amplifier (OP-AMP) circuits can be used to
- D. Neither inverting nor non-inverting Operational Amplifier (OP-AMP) circuits can be used to

5. The output for this component is the integral of the input. It is also used for Low pass filter circuits and sensor conditioning circuits. What type of Operational Amplifier (OP-AMP) does this statement refer to? [CLO 1]
- A. Inverting
 - B. Non inverting
 - C. Integrator
 - D. Differentiator
6. A voltage summing amplifier has _____. [CLO 1]
- A. several inputs and several outputs
 - B. several inputs and one output
 - C. one input and several outputs
 - D. one input and one output
7. A timer is connected in astable mode. Calculate the Time High when $R_1 = 8 \text{ k}\Omega$, $C_1 R_2 = 2.5 \text{ k}\Omega$ and $= 0.1 \text{ }\mu\text{F}$ are given $C = 0.01 \text{ }\mu\text{F}$ is used as a noise diverter. [CLO 1]
- A. 0.70 ms
 - B. 0.72 ms
 - C. 0.74 ms
 - D. 0.76 ms
8. The function of a high pass filter is to allow _____ frequency signal to pass through and attenuates the frequency _____ the cut off point. [CLO 1]
- A. low , above
 - B. high, below
 - C. low, below
 - D. high, above

9. Which of the following is a low pass filter?

[CLO 1]



10. The function of an analog to digital converter is to change the _____ signal to the _____ signal.

[CLO 1]

- A. analog, digital
- B. analog, analog
- C. digital, analog
- D. digital, digital

SECTION A2: FILL IN THE BLANKS (10 Questions)

11. Complete the block diagram of a DC power supply marked Z in Figure 2. [CLO 1]

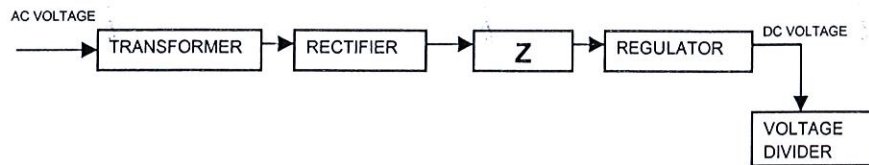


Figure 2

12. The Filter circuit is used in DC power supply to convert the _____ to the _____. [CLO 1]
13. Only if the condition of $\beta A =$ _____ is satisfied, the self-sustained oscillations can function. [CLO 1]
14. The comparator is considered a _____ loop Operational Amplifier (Operational Amplifier (OP-AMP)) circuit. [CLO 1]
15. The most common IC for Operational Amplifier (OP-AMP) is Integrated Circuit (IC) _____. [CLO 1]
16. CMRR stands for _____. [CLO 1]
17. The Timer 555 consists of two _____, a flip-flop, a discharge transistor and a resistive voltage divider. [CLO 1]
18. The _____ is also known as *notch*. [CLO 1]
19. In analyzing filters, the _____ unit is often used to describe the amount of attenuation offered by the filter. [CLO 1]
20. The resolution of a Digital Analogue Converter (DAC) or Analogue Digital Converter (ADC) specifies the _____. [CLO 1]

SECTION B : STRUCTURED (10 Questions)

Instruction: This section consists of **TEN (10)** subjective questions. Write your answer in the answer booklet.

QUESTION 1

List **THREE (3)** types of regulator circuit.

[CLO 1]

(3 marks)

QUESTION 2

Explain the function of a rectifier. Draw the input and output waveforms for the full wave rectifier.

[CLO 1]

(3 marks)

QUESTION 3

State **THREE (3)** types of Sinusoidal Oscillator circuit.

[CLO 1]

(3 marks)

QUESTION 4

Given that $C_1=10\mu\text{F}$ and $C_2=0.47\mu\text{F}$, what is the resonant frequency for Colpitts Oscillator.

[CLO 1]

(3 marks)

QUESTION 5

Determine the close loop voltage gain for Figure 3 below.

[CLO 1]

(3 marks)

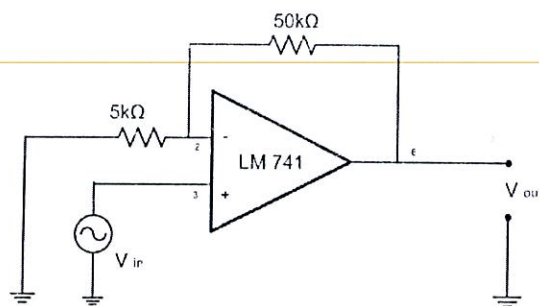


Figure 3

QUESTION 6

State the differences between Astable and Bistable multivibrator mode in Timer 555 IC. [CLO 1]
(3 marks)

QUESTION 7

The timer 555 is connected in monostable multivibrator mode. [CLO 1]
Determine the duration of output pulse when the value of $R=10\text{ k}\Omega$ and $C=0.1\text{ }\mu\text{F}$. (3 marks)

QUESTION 8

Calculate the cut-off frequency of an active low pass filter with [CLO 1]
 $R=50\Omega$ and $C=0.01\text{ }\mu\text{F}$. (3 marks)

QUESTION 9

Draw a filter circuit for [CLO 1]
i. Passive Low Pass Filter (3 marks)
ii. Active Low Pass Filter

QUESTION 10

Briefly explain the differences between A/D converter and D/A converter. [CLO 1]
(3 marks)

SECTION C : ESSAY (2 Questions)

Instruction: This section consists of **TWO [2]** essay questions. Answer **all** questions.

QUESTION 1

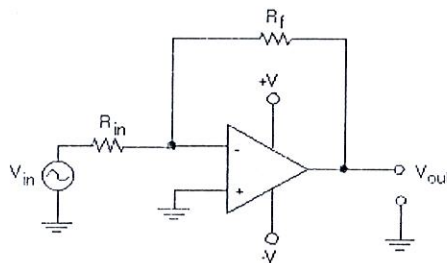
- (a) The open-loop gain of a certain Operational Amplifier [CLO 1]
(Operational Amplifier (OP-AMP)) is 100,000. Its common-mode
gain is 0.2. Determine the CMRR in decibels. (6 marks)

- (b) Define input bias current and input offset current. [CLO 1]

Determine the bias current, I_{BIAS} , given that the input currents to an (7 marks)
Operational Amplifier (OP-AMP) are 8.3 mA and 7.9mA.

- (c) Based on inverting amplifier in Figure 4 [CLO 1]

- (i) Determine the closed loop gain (12 marks)
- (ii) If a signal voltage of 10mVp is applied, determine the output
voltage.
- (iii) Draw the phase relationship of input and output voltages.



Given $R_f = 330 \text{ k}\Omega$

$R_{in} = 33 \text{ k}\Omega$

Figure 4

QUESTION 2

a) (i) Draw the schematic diagram of Timer 555 for a monostable [CLO 1]

(4 marks)

(ii) Briefly explain the function of pin-2 and pin-4 in Timer 555 configuration. [CLO 1]

(4 marks)

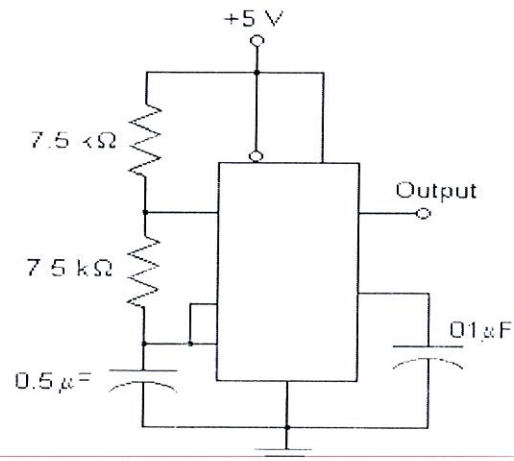


Figure 5

b) Based on Figure 5, a Timer 555 is connected in astable mode. [CLO 1]

1. Determine

(10 marks)

- i. Time High (T_H)
- ii. Time Low (T_L)
- iii. Frequency (f)
- iv. Duty cycle (%D)

2. Sketch the waveform at pin-3 and pin-6 for the Timer 555

c) Give the definition of the term below [CLO 1]

i. Resolution (4 marks)

ii. Step size

d) Sketch the schematic circuit for the R-2R Ladder DAC circuit in [CLO 1]

the Digital to Analog Converter process. (3 marks)