POLITEKNIK
Jabatan Pengajian Politeknik

EXAMINATION AND EVALUATION DIVISION
DEPARTMENT OF POLYTECHNIC EDUCATION
(MINISTRY OF HIGHER EDUCATION)

ELECTRICAL ENGINEERING DEPARTMENT

FINAL EXAMINATION

JUNE 2012 SESSION

EC303: COMPUTER ARCHITECTURE AND ORGANIZATION

DATE :22nd NOVEMBER 2012 (THURSDAY)
DURATION : 2 HOURS (11.15AM – 1.15PM)

This paper consists of TWELVE (12) pages including the front page.
Section A1 : Objective (10 Question)
Section A2 : Fill in the blank (10 Question)
Section B : Structure (10 Question)
Section C : Essay (2 Question)
Answer all questions.

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(The CLO stated is for reference only)

~~SECTION A (20 MARKS)~~

SECTION A1: OBJECTIVE (QUESTION 1 – QUESTION 10)

Instruction: This section consists of **TEN (10)** objective questions. Write your answer's in the answer booklet.

1. Which of the following are functionally independent main parts of basic CPU Organization?

CLO 1

i. Arithmetic and Logic
ii . Memory
iii. Control
iv. ROM

A. i,ii and iv
B. ii,iii and iv
C. i,ii and iii
D. i,iii and iv

2. There are FOUR (4) common types of shift registers. Which one is false?

CLO 2

A. Serial in – serial out
B. Parallel in – serial out
C. Serial in – latch out
D. Parallel in – parallel out

3. The _____ is the part of the CPU that actually performs arithmetic and logical operations on data.

CLO 2

A. ALU
B. ASCII
C. IC
D. RAM

4. What are the parts of an instruction cycle ?

CLO 2

A. Fetch and Execute Cycle
B. Fetch, decode and execute cycles
C. Decode and Store cycle
D. Fetch, decode, execute and store

5. Solve the addition of $110111_2 + 101100_2$ and convert it to the decimal number. CLO 2

A. 89
B. 99
C. 79
D. 69

6. _____ is one of the output of ALU. CLO 2

A. Adder Component
B. Shift Register
C. Flag register
D. Timing Diagram

7. Which are **TRUE** about Half Adder CLO 2

i. combinational circuit that performs the addition of two bits
ii. accepts two binary digits on its inputs and produce two binary digits outputs, a sum bit and a carry bit.
iii. performs the addition of three bits (two significant bits and a previous carry)
iv. combinational circuit that forms arithmetic sum off three input bits.

A. i and ii
B. i and iv
C. i,ii and iii
D. iii and iv

8. What type of Shift Register is in Figure 1?

CLO 2

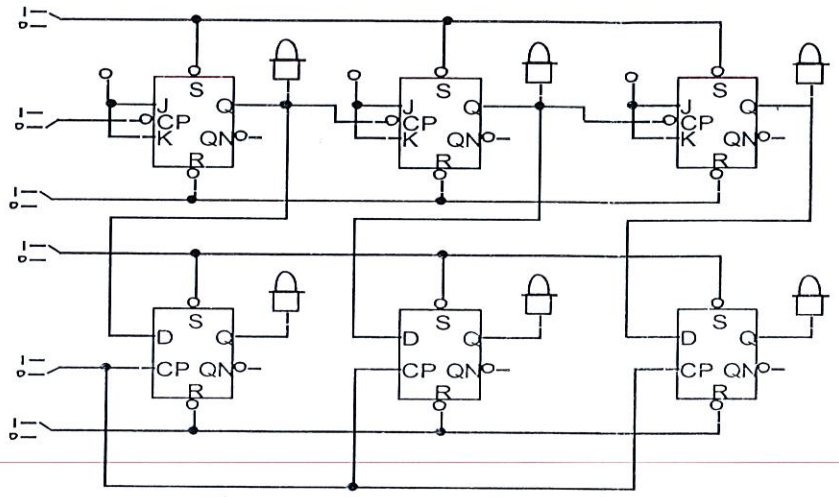


Figure 1

series

A. Parallel shift register
B. Series shift register
C. Series-parallel shift register
D. Parallel shift register

9. The following statements are true about Memory Mapped I/O EXCEPT

CLO 3

A. A separate code or control signal based on the op code will select either memory or I/O
B. Higher order addresses can refer to device
C. Lower order addresses can refer to Memory
D. Device or memory selection based on address range

10. Universal Serial Bus (USB) was designed to standardize the connection of computer peripherals to personal computer, to communicate and also to supply electric power. Which is the standard connector available for USB?
CLO 3

i. Standard-A Plug
ii. Standard-B Plug
iii. Standard-A Receptacle
iv. Standard-B Receptacle

A. i and ii
B. i and iii
C. i, ii and iii
D. All the Above

SECTION A2 : FILL IN THE BLANKS (QUESTION 11 – QUESTION 20)

Instructions: This section consists of **TEN (10)** fill in the blanks questions. Write your answer's in the answer booklet.

11. Computer _____ encompasses all physical aspects of computer systems.

CLO 1

12. Computer _____ is the logical aspects of system implementation as seen by the programmer.

CLO 1

13. _____ is one of the primary approaches to IC chip design.

CLO 2

14. The negative numbers in the binary system can be represented by _____.

CLO 2

15. An instruction _____ is a technique used in the design of computers and other digital electronic devices to increase their instruction throughput (the number of instructions that can be executed in a unit of time).

CLO 2

16. _____ is a combinational circuit that receives binary information from one of 2^n input data lines and directs it to a single output line.

CLO 2

17. The major difference between half-adders and full adders is, _____ have a carry input capability.

CLO 2

18. Main memory locations can only be copied into one location. This is accomplish by dividing main memory into _____ that correspond with the size of the cache.

CLO 3

19. The advantages of Direct Memory Access (DMA), computer system performance is improved by direct transfer data between _____ devices, by passing the CPU.

CLO 3

20. Universal Serial Bus (USB) was designed to standardize the connection of _____ to personal computer, to communicate and also to supply electric power.

CLO 3

STRUCTURE (10 QUESTIONS)

Instruction: This section consists of **TEN (10)** structured questions.Answer **ALL** questions.

Question 1

State the main electronic component used in first generation and second generation of computers respectively.

CLO1
(3 marks)

Question 2

Draw the truth table for the master-slave J-K flip-flop.

CLO2
(3 marks)

Question 3

Draw the block diagram of Von Neumann's computer architecture system.

CLO2
(3 marks)

Question 4

Convert 0.81_{10} to binary number.

CLO2
(3 marks)

Question 5

Describe the operations of ALU.

CLO2
(3 marks)

Question 6

Sketch the diagram of binary half adder.

CLO2

(3 marks)

Question 7

Draw the memory hierarchy block diagram.

CLO3
(3 marks)

Question 8

Explain the virtual memory segmented system.

CLO3
(3 marks)

Question 9

Illustrate a DMA transfer between RAM and the peripheral device.

CLO3
(3 marks)

Question 10

List **THREE (3)** basic functions of the USB host.

CLO3
(3 marks)

SECTION C

ESSAY (2 QUESTIONS)

Instruction: This section consists of **TWO (2)** essay questions. Answer **ALL** questions.

QUESTION 1

a) ALU is the part of the computer that actually performs arithmetic and logical operations on data. List 2 (TWO) main functions of the ALU.

CLO 2

(4 marks)

b) The adder is a major component of an Arithmetic Logic Unit (ALU) in a CPU. A full adder is a logical circuit that performs an addition operation on three binary digits.

S = (A XOR B) XOR Ci
Co = (A AND B) OR (Ci AND (A XOR B))

Based on the above Boolean equation ,

i. Draw a block diagram of full adder.

CLO 2

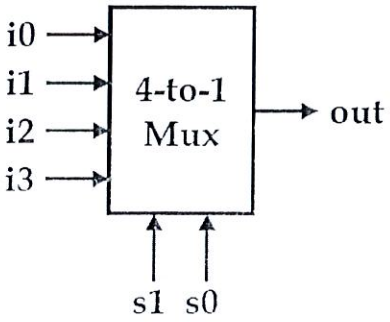
(4 marks)

ii. Sketch the logic schematic of a full adder.

CLO 2

(8 marks)

c) In electronics, a multiplexer (MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line.



s1	s0	out
0	0	i0
0	1	i1
1	0	i2
1	1	i3

Figure 1: Block diagram and truth table of 4-to-1 MUX

Based on the given statement above:

i. Where the MUX been applied? State 1 (ONE) of the MUX application.

CLO 2

(1 mark)

ii. Explain on how the multiplexer works.

CLO 2

(4 marks)

iii. Based on the Figure 1, state the Boolean equation for each of the output.

CLO 2

(4 marks)

QUESTION 2

a) Draw a block diagram that shows a typical interconnection in computer systems.

CLO3
(5marks)

b) Give **THREE (3)** advantages of single bus system and sketch a suitable figure of this system.

CLO3
(6 marks)

c) Why are tristate buffers required to interface digital devices to a bus? Draw a block diagram of this logic circuit and truth table of Active High tristate buffer.

CLO3
(10 marks)

d) Sketch the diagram of USB system design. CLO3
(4 marks)